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Intelligent Automation Incorporated

Coherent distributed radar for high-resolution through-wall imaging

SBIR Phase I Progress Report 2

Contract No. N00014-10-C-0277

Sponsored by

Office of Naval Research

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1.0 SUMMARY

In this performance we continued developing an overall plan for design of RF transceiver hardware for very accurate synchronization. Selection of key hardware components, such as a highly accurate reference clock has been narrowed down a few candidates. A meeting with the ONR client, and SAIC staff to kickoff the project was held.

1.1 Introduction

In this report we discuss progress in hardware design, synchronization algorithm, and definition of the final demonstration.

1.2 Synchronization algorithm

An analytical signal level description of the synchronization algorithm has been defined. We are now starting to design a Matlab simulation of the algorithm. The Matlab code will be used to evaluate performance under multipath conditions, hardware limitations, noise and interference. The Matlab cod will also be used to estimate required resources; the estimate will guide selection of the system FPGA.

1.3 Hardware design

In the previous period we had identified a very high accuracy reference clock that has very high cost (~$2K), long lead time (~6 months), and is available from only one vendor. In this period we have determined that reference clocks with somewhat higher levels of phase noise may be used without affecting the final synchronization accuracy. We have identified three potential candidate reference clocks and will analyze the data sheets further, perform simulations, and perform bench top measurements on samples to determine which one will be used in our design.

1.3 Kickoff Meeting

On May 14, 2010, a kickoff meeting was held at the MTCSC facility in Stafford, VA. Present were Andre des Rosiers (NRL/ONR), Leon Elam (SAIC), Martin Kruger (ONR), Ted Isaacson form ITSFAC, and Eric van Doorn and Charles Abraham from IAI. We discussed progress made to date, the schedule, and expectations and intended audience for the combined demonstration of bi-static synchronized through-wall radar in FY11. We also discussed how IAI and SAIC will collaborate to make the demonstration a success. SAIC is currently tasked to develop 1 radar prototype, while at least two radars would be needed to demonstrate improved cross-range resolution due to synchronized bi-static operation. One option to avoid use of a second unit is to use a table top equipment-based transmitter in lieu of the second radar. We determined that the frequency plans for the through-wall radar and synchronization transceiver are mutually compatible. We also determined that SAIC will provide IAI with specifications for the synchronization signals that will be provided to the radar unit(s), including: system clock frequency, system clock signal level, trigger signal rise time and signal level, impedance of traces, pins, connectors or cables to physically interface to the radar.

Our understanding is that:

1. In FY10, IAI focus will be on designing and building the synchronizing transceiver.
2. Demonstration will be held early/middle in FY11, exact date and location TBD. The audience for the demonstration has not been defined but would include members from the S&T community.

3. Demonstration will involve 2 radar units, or 1 radar unit and a table top transmitter, synchronized by IAI hardware to within 1/5-1/10 of smallest wavelength scattered from behind-wall target and detected by the radar.

4. Ranges between radar units are about 50-100ft.

5. Radar antennas located by means of differential GPS and angle sensors by IAI with accuracy compatible with synchronization accuracy. Radar units will be stationary or move minimally.

6. How bi-static radar data is stored, acquired, processed, and visualized has not been determined yet.

2.0 FINANCIALS

Period of Performance: 3/18/2010 – 9/18/2011
Contract value: $515,168
Funded value: $320,000
Cost incurred as of 5/11/2010: $30,483.82

3.0 CONCLUSIONS AND WORK PLANNED FOR NEXT REPORTING PERIOD

We have now detailed a mathematical description of the synchronization algorithm. Next in our design efforts is to translate this description into a Matlab algorithm to evaluate performance under the effects of temperature variations, multipath, interference, and hardware non-idealities such as noise. The Matlab implementation will also be used to accurately determine the resources needed in the FPGA that will perform the signal generation, signal acquisition, and digital processing, and narrow down selection of the system FPGA.

We have defined the overall clocking scheme, and identified candidates for key components, such as a high-precision reference clock. In the next period, we will select the reference clock. We have partially completed schematics of the RF front-end and will be able to estimate the sensitivity, dynamic range, and noise figure of the proposed design in the next reporting period. Key characteristics of the proposed hardware design, such as jitter, internal delays, and noise figure will be tabulated to provide an overall noise figure to be incorporated in the Matlab simulation of the synchronization algorithm.

4.0 REFERENCES

None.

5.0 LIST OF SYMBOLS, ABBREVIATIONS, AND ACRONYMS

None.